REMARKS/ARGUMENTS

Claims 1-32 are pending in the present application.

This Amendment is in response to the Office Action mailed November 5, 2003. In the Office Action, the Examiner rejected claims 1-32 under 35 U.S.C. §112; and claims 1-32 under 35 U.S.C. §103(a). Applicant has amended claims 1, 4, 14, 17, 27 and 30. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 112

1. In the Office Action, the Examiner rejected claims 1-32 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant has amended claims 1, 14, and 27 to clarify the claim language.

Therefore, Applicant respectfully requests the rejection under 35 U.S.C. §112 be withdrawn.

Rejection Under 35 U.S.C. § 103

1. In the Office Action, the Examiner rejected claims 1-2, 14-15, and 27-28 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,237,064 issued to Kumar et al. ("Kumar") in view of U.S. Patent No. 6,629,218 issued to Cho ("Cho") and claims 3-13, 16-26, and 29-32 under 35 U.S.C. §103(a) as being unpatentable over Kumar in view of Cho and further in view of U.S. Patent No. 6,438,657 issued to Gilda ("Gilda"). Applicant respectfully traverses the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of obviousness.

Applicant reiterates the arguments set forth in the previously filed Response to the Office Action.

Kumar discloses a cache memory with reduced latency by paralleling various memory accesses initiated by the execution unit (Kumar, col. 3, lines 42-44). A first cache, a second cache, and a tag array of a third cache are resident in the processor core (Kumar, col. 3, lines 9-13).

Cho discloses an out of order associative queue in two clock domains. A system includes two processors, an L2 cache, a memory controller, a pair of input/output (I/O) bridges, and I/O

interfaces (Cho, col. 3, lines 14-16). The processors, the L2 cache, the memory controller, the I/O interfaces, the I/O bridges, and the bus may be integrated onto a single integrated circuit as a system on a chip configuration (Cho, col. 5, lines 38-42). Any level of integration may be used (Cho, col. 5, line 47).

Gilda discloses a pipelined snooping of multiple L1 cache lines. An L2 cache control unit provides the processor with access to a private L2 cache (Gilda, col. 11, lines 55-61).

Kumar, Cho and Gilda, taken alone or in any combination, does not disclose, suggest, or render obvious controlling cache memory in an external chipset via double-pumped or quad-pumped control signals.

There is no motivation to combine Kumar, Cho and Gilda because neither of them addresses the problem of controlling cache memory in an external chipset. There is no teaching or suggestion that double-pumped or quad-pumped control signals are present. Kumar, read as a whole, does not suggest the desirability of controlling cache memory in an external chipset via double-pumped or quad-pumped control signals.

To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 USPQ (BNA) 543, 551 (Fed. Cir. 1985). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the Examiner must show reasons that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the prior elements from the cited prior references for combination in the manner claimed. In re ROUFFET, 149 F.3d 1350 (Fed. Cir. 1996), 47 USPQ 2d (BNA) 1453. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985).

In the present invention, the cited references do not expressly or implicitly suggest controlling cache memory in an external chipset via double-pumped or quad-pumped control

signals. In addition, the Examiner failed to present a convincing line of reasoning as to why a combination of Kumar, Cho and Gilda is an obvious application of controlling cache memory in external chipset.

Therefore, Applicant believes that independent claims 1, 14, 27 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejections under 35 U.S.C. §112, and 35 U.S.C. §103(a) be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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Dated: 01/12/2004 By _____

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